WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a write signal line to transmit write data;

a write column selection switch being possible to transmit said write data on said write signal line to a bit line;

a write column selection line supplying an operation control signal to said write column selection switch;

a sense amplifier column comprising a plurality of sense amplifier circuits to amplify read data which are read to said bit line from a memory cell;

a read signal line to transmit read data;

a read column selection switch to selectively transmit the read data of said bit line to said read signal line;

a read column selection line supplying an operation control signal to said read column selection switch; and

a control circuit to control operations of said write column selection switch and read column selection switch in different timings,

wherein said write signal line and said read signal line are allocated crossing said sense amplifier column and said write column selection line and said read column selection line are allocated in parallel to said sense amplifier column.

2. The semiconductor memory device according to claim 1,

wherein said sense amplifier circuit comprises a write amplifier section to drive said bit line based on the data of said write signal line and a read amplifier section to drive said read signal line based on the data of said bit line,

wherein said write column selection line is provided using a wiring layer in the area where said write amplifier section is formed, and

wherein said read column selection line is provided using a wiring layer in the area where said read amplifier section is formed.

3. The semiconductor memory device according to claim 2, wherein a sense amplifier section to amplify the read data is allocated between said write amplifier section forming area and said read amplifier section forming area.

4. A semiconductor memory device comprising:

a write signal line to transmit write data;

a column selection switch for write to transmit said write data transmitted via said write signal line to a bit line;

a column selection line for write to supply an operation control signal to said column selection switch for write;

a sense amplifier column comprising a plurality

of sense amplifier circuits to amplify the read data which is read to the bit line from memory cells;

a read signal line to transmit read data;

a column selection switch for read to selectively transmit said read data of said bit line to said read signal line;

a column selection line for read to supply an operation control signal to said column selection switch for read;

a control circuit to control operations of said column selection switch for write and said column selection switch for read in different timings; and

a precharge circuit to precharge said read signal line,

wherein said control circuit comprises a logical circuit to control said column selection switch for read to the OFF state from the ON state after the precharge operation of said read signal line is started.

5. The semiconductor memory device according to claim 4, wherein said logical circuit includes a column decoder to generate an operation control signal of said column selection switch for read based on a column address signal.

6. A semiconductor memory device, comprising:

a read signal line for data read;

a main amplifier to fetch and amplify the data of said read signal line;

a precharge circuit to precharge said read signal line; and

a circuit to control start of a precharge operation of said read signal line with said precharge circuit after the operation of said main amplifier is started.

7. The semiconductor memory device according to claim 6, comprising:

a write signal line to transmit write data;

a column selection switch for write to transmit said write data transmitted via said write signal line to bit lines;

a column selection line for write to supply an operation control signal to said column selection switch for write;

a sense amplifier column formed of a layout of a plurality of sense amplifier circuits to amplify read data which are read to the bit lines from memory cells;

a read signal line for transmitting read data;

a column selection switch for read to selectively transmit the read data of said bit lines to said read signal line;

a column selection line for read to supply an operation control signal to said column selection switch for read; and

a control circuit to control operations of said column selection switch for write and said column selection switch for read in different timings.

8. The semiconductor memory device according to claim 7, wherein said control circuit comprises a means to control said column selection switches to the OFF state from the ON state after the precharge operation of said read signal line is started with said precharge circuit.

9. The semiconductor memory device according to claim 7, wherein said control circuit comprises a means to control said column selection switches to the OFF state from the ON state almost simultaneously with start of the precharge operation of said read signal line by said precharge circuit.